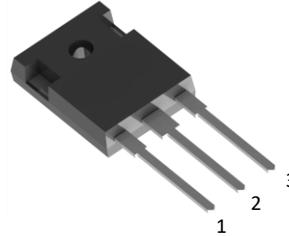
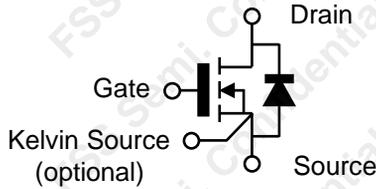


Silicon Carbide MOSFET

1200V, 40mΩ SiC MOSFET – Falcon Series



Product Information:



TO-247-3L



TO-247-4L

Features

- Optimized $R_{DS(on)}$ with Rapid Switching Behavior
- Compatible with Standard Gate Drivers
- Clean Kelvin-Source Switching Pin-out (4L type)
- 8mm of Drain to Source Creepage Distance (4L type)
- High Avalanche Endurance Capability
- Optimized for High Power Density Applications
- RoHS Compliant and Halogen Free

Benefits

- Higher System Efficiency
- Increase Parallel Device Convenience
- Enable High Temperature Application
- Allow High Frequency Operation
- Realize Compact and Lightweight Systems
- High Reliability

Terminal	Packaging Type	
	TO-247-3L	TO-247-4L
Gate	1	4
Drain	2, Tab	1, Tab
Source	3	2
Kelvin Source	--	3

Potential Applications

- Switching Mode Power Supply
- PFC & DC/DC Converter
- EV Charging Station
- UPS
- Renewable Energy
- Power Inverter & Motor Driver

Key Performance Parameters

Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS} @ T_{j(max)}$	1200	V
Recommended Gate-Source Turn-On Voltage	V_{GS}	15~18	
Drain-Source On-State Resistance	$R_{DS(on)}$	40	mΩ
Continuous Drain Current	I_D	47	A
Pulse Drain Current	$I_{D, pulse}$	128	
Power Dissipation	P_{tot}	202	W
Avalanche Energy	E_{AS}	800	mJ
Gate Charge	Q_G	117	nC
Output Capacitive Charge	Q_{oss}	140	
Junction & Storage Temperature	T_j, T_{stg}	-55 to 175	°C

Part Number	Package	Marking
FF12040E-3	TO-247-3L	FF12040
FF12040Q	TO-247-4L	FF12040

For further information about comparable products, please contact (www.fastsic.com).

Maximum Ratings: ($T_j = 25^\circ\text{C}$, unless otherwise specified)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Drain-Source Voltage	V_{DSS}	1200	--	--	V	$V_{GS}=0\text{V}, I_D=5\text{mA}$
Continuous Drain Current	I_D	--	--	47 35	A	$V_{GS}=18\text{V}, T_c=25^\circ\text{C}$ $V_{GS}=18\text{V}, T_c=100^\circ\text{C}$
Pulse Drain Current	$I_{D, pulse}$	--	--	128		Per Fig. 12
Continuous Body Diode Current	I_S	--	--	37		$V_{GS}=0\text{V}, T_c=25^\circ\text{C}$
Avalanche Energy, Single Pulse	E_{AS}	--	--	800	mJ	$L=25\text{mH}$
Operate Gate Source Voltage	$V_{GS, op}$	-8~0	--	15~18	V	Recommended operating values
Transient Gate Source Voltage	$V_{GS, tran.}$	-10	--	22		Transient operating limit ($AC f > 1\text{Hz}$, pulse width $< 100\text{ns}$)
Power Dissipation	P_{tot}	--	--	202	W	$T_c=25^\circ\text{C}$
Junction Temperature	T_j	-55	--	175	°C	--
Storage Temperature	T_{stg}	-55	--	175		
Soldering Temperature	T_L	--	--	260		

Electrical Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions	
DC Characteristics (at $T_j = 25^\circ\text{C}$, unless otherwise specified)							
Drain-source Breakdown Voltage	$V_{(BR)DSS}$	1200	-- 1200	--	V	$V_{GS}=0\text{V}, I_D=5\text{mA}, T_j=25^\circ\text{C}$ $V_{GS}=0\text{V}, I_D=5\text{mA}, T_j=175^\circ\text{C}$	
Drain-Source On-State Resistance	$R_{DS(on)}$	--	40 68	56	mΩ	$V_{GS}=18\text{V}, I_D=20\text{A}, T_j=25^\circ\text{C}$ $V_{GS}=18\text{V}, I_D=20\text{A}, T_j=175^\circ\text{C}$	
Gate-Source Threshold Voltage	V_{th}	--	2.2	--	V	$V_{GS}=V_{DS}, I_D=40\text{mA}$	
Zero Gate Voltage Drain Current	I_{DSS}	--	2	500	μA	$V_{DS}=1200\text{V}, V_{GS}=0\text{V}, T_j=25^\circ\text{C}$	
Gate-Source Leakage Current	I_{GSS}	--	--	100	nA	$V_{GS}=18\text{V}, V_{DS}=0\text{V}$	
Body Diode Forward Voltage	V_{SD}	--	3.1 3.0	--	V	$V_{GS}=0\text{V}, I_S=15\text{A}, T_j=25^\circ\text{C}$ $V_{GS}=0\text{V}, I_S=15\text{A}, T_j=175^\circ\text{C}$	
AC Characteristics (at $T_j = 25^\circ\text{C}$, unless otherwise specified)							
Input Capacitance	C_{iss}	--	3129	--	pF	$V_{DS}=800\text{V}, V_{GS}=0\text{V},$ $f=250\text{kHz}, V_{AC}=25\text{mV}$	
Output Capacitance	C_{oss}	--	95	--			
Reverse Capacitance	C_{rss}	--	13	--			
Effective Output Capacitance, energy related	$C_{o(er)}^1$	--	123	--			
Effective Output Capacitance, time related	$C_{o(tr)}^2$	--	175	--			
C_{oss} Stored Energy	E_{oss}	--	39	--			μJ
Output Capacitive Charge	Q_{oss}	--	140	--			nC
Internal Gate Resistance	$R_{G, int.}$	--	2.4	--	Ω	$f=1\text{MHz}, V_{AC}=25\text{mV}$	

¹ $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 800V.

² $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 800V.

Switching Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Gate Characteristics						
Gate to Source Charge	Q_{GS}	--	22	--	nC	$V_{DS}=800V, V_{GS}=0V/15V, I_D=40A$
Gate to Drain Charge	Q_{GD}	--	52	--		
Total Gate Charge	Q_G	--	117	--		
Inductive Load						
Turn On Delay Time	$t_{d(on)}$	--	47	--	ns	$V_{DS}=800V,$ $I_D=35A,$ $V_{GS}=-3/+15V,$ $R_{G(ext.)}=2.7\Omega$ External SiC Diode as an FWD
Rise Time	t_r	--	52	--		
Turn Off Delay Time	$t_{d(off)}$	--	28	--		
Fall Time	t_f	--	11	--		
Turn On Switching Energy	E_{on}	--	739	--	μJ	External SiC Diode as an FWD
Turn Off Switching Energy	E_{off}	--	61	--		
Resistive Load						
Turn On Delay Time	$t_{d(on)}$	--	22	--	ns	$V_{DS}=800V,$ $I_D=26A, V_{GS}=-3/+15V,$ $R_{G_{on, ext.}}=2.7\Omega, R_{G_{off, ext.}}=1\Omega$ $R_L=30\Omega,$
Rise Time	t_r	--	29	--		
Turn Off Delay Time	$t_{d(off)}$	--	32	--		
Fall Time	t_f	--	11	--		
Body Diode Characteristics						
Reverse Recovery Charge	Q_{rr}	--	98	--	nC	$V_{GS}=0V,$ $I_S=30A, V_{DS}=400V,$ $di/dt=300A/\mu s$ * Q_{rr} herein excluded the Q_{oss} value.
Reverse Recovery Time	t_{rr}	--	60	--	ns	
Peak Reverse Recovery Current	I_{rrm}	--	3.0	--	A	

Thermal Characteristics:

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Thermal Impedance, junction-case	R_{th-jc}	--	0.74	--	K/W	--
Thermal Impedance, junction-ambient	R_{th-ja}	--	40	--		Device on PCB, with 6 cm ² of cooling area

Electrical Characteristics Diagrams

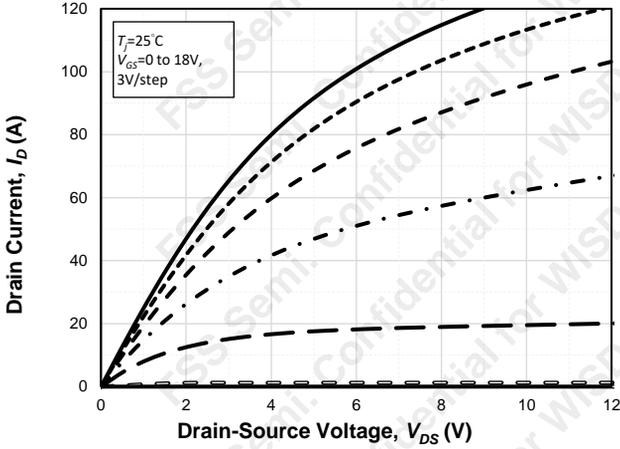


Fig. 1 Typical Output Characteristics at $T_j=25^\circ\text{C}$

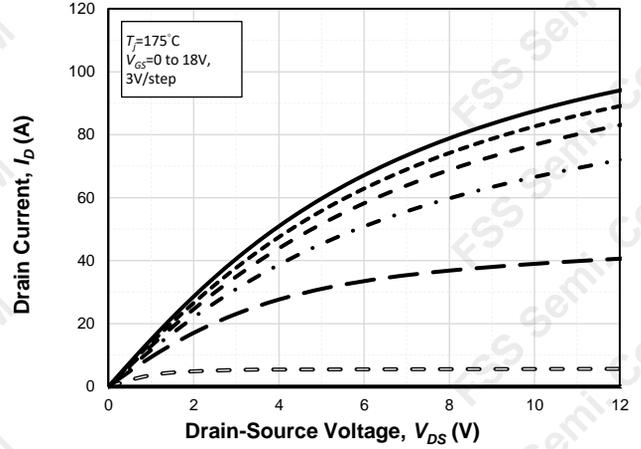


Fig. 2 Typical Output Characteristics at $T_j=175^\circ\text{C}$

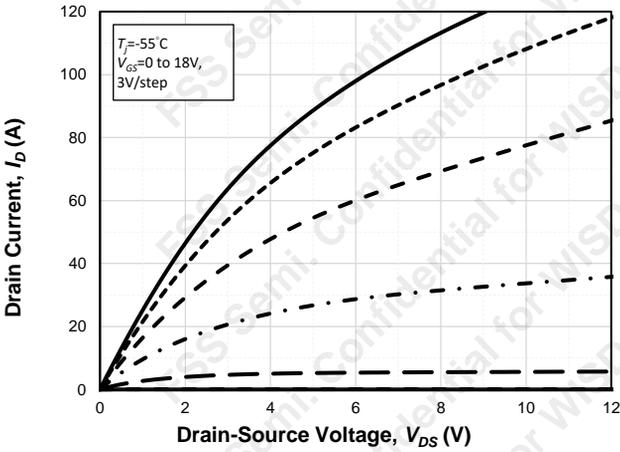


Fig. 3 Typical Output Characteristics at $T_j=-55^\circ\text{C}$

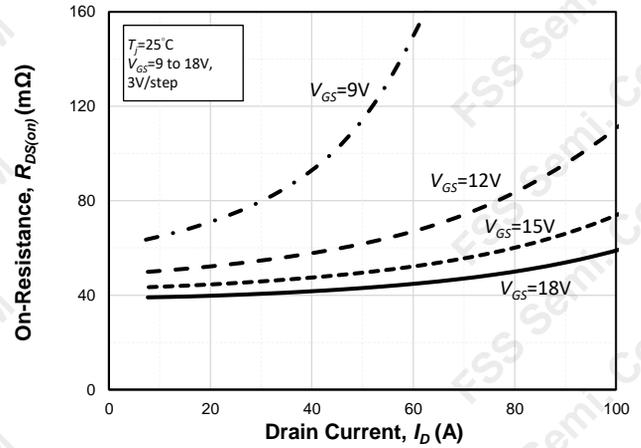


Fig. 4 Typ. $R_{DS(on)}$ vs. I_D with Various V_{GS}

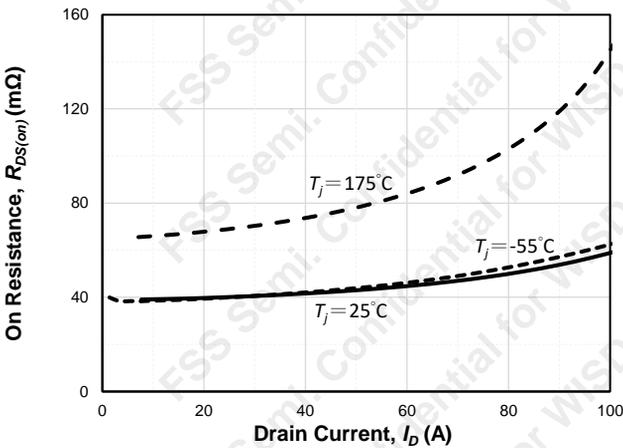


Fig. 5 Typ. I_D vs. V_{GS} with Various T_j , $V_{DS}=10\text{V}$

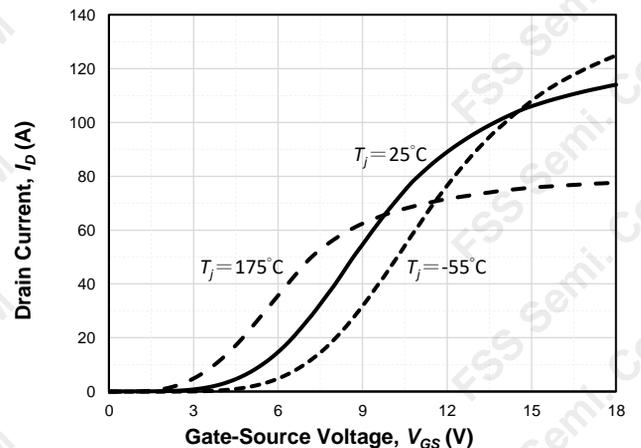


Fig. 6 Typ. I_D vs. V_{GS} with Various T_j , $V_{DS}=10\text{V}$

Electrical Characteristics Diagrams

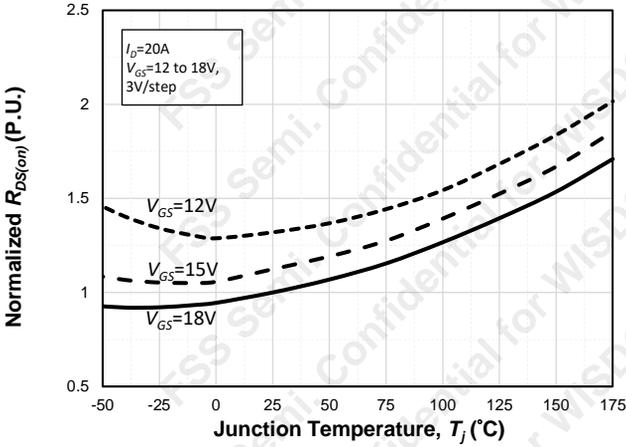


Fig. 7 Normalized $R_{DS(on)}$ vs. T_J with Various V_{GS}

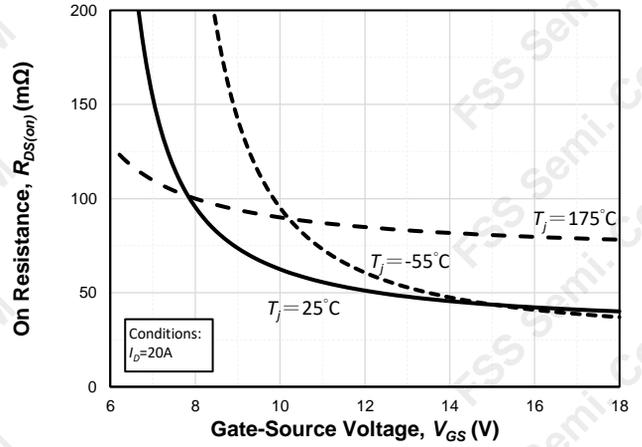


Fig. 8 Typ. $R_{DS(on)}$ vs. V_{GS} with Various T_J

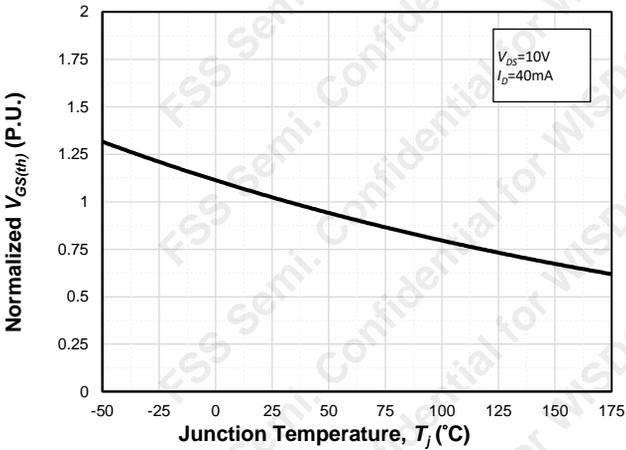


Fig. 9 Normalized V_{th} vs. T_J

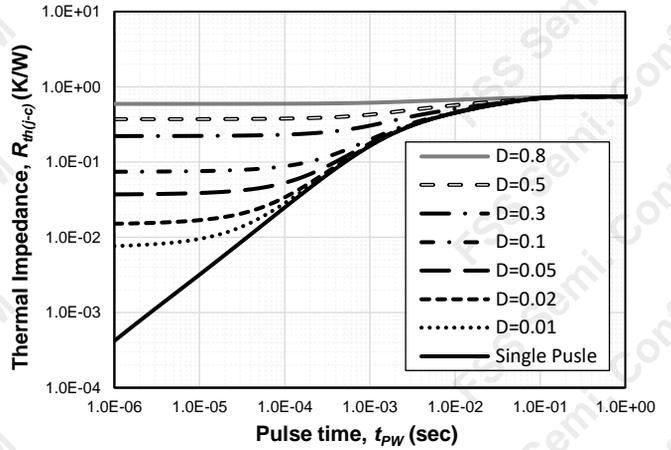


Fig. 10 Typ. Transient Thermal Impedance R_{th-jc}

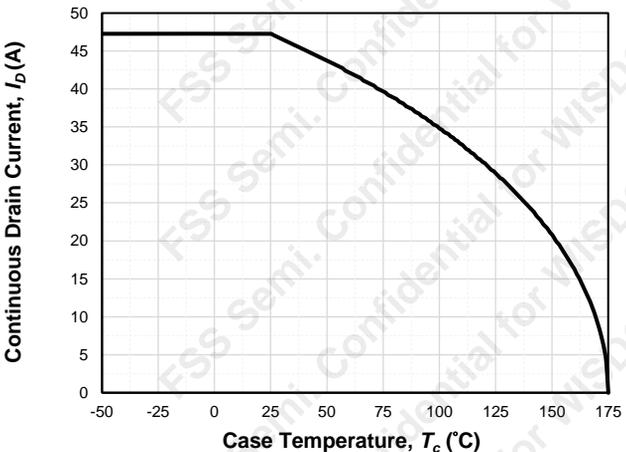


Fig. 11 Continuous I_D De-rating at $V_{GS}=18V$, $T_J \leq 175^\circ C$

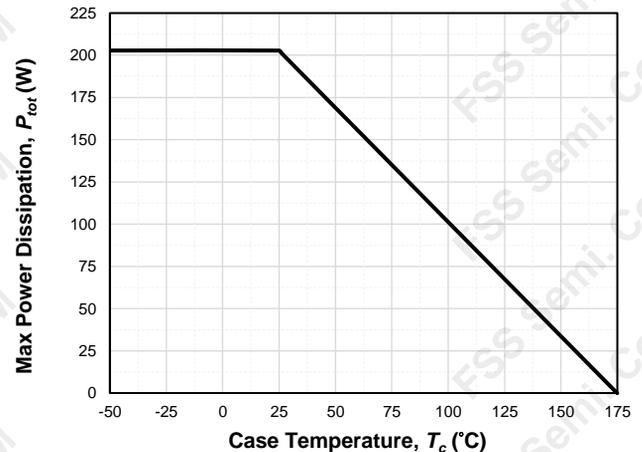


Fig. 12 Power Dissipation at $V_{GS}=18V$, $T_J \leq 175^\circ C$

Electrical Characteristics Diagrams

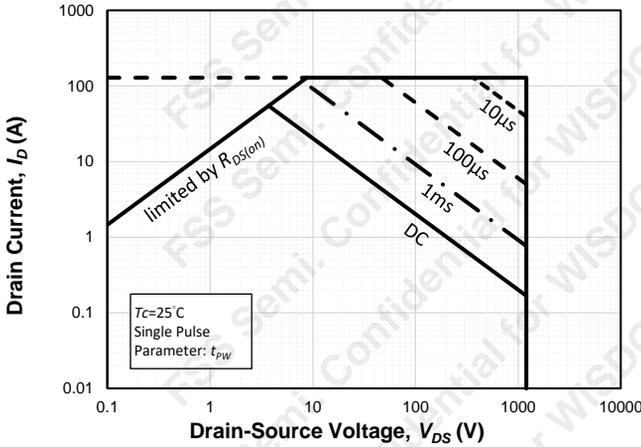


Fig. 13 Safe Operating Area at $T_c = 25^\circ\text{C}$

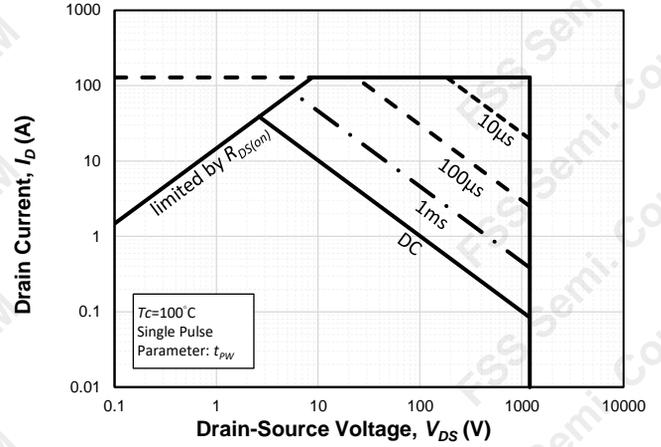


Fig. 14 Safe Operating Area at $T_c = 100^\circ\text{C}$

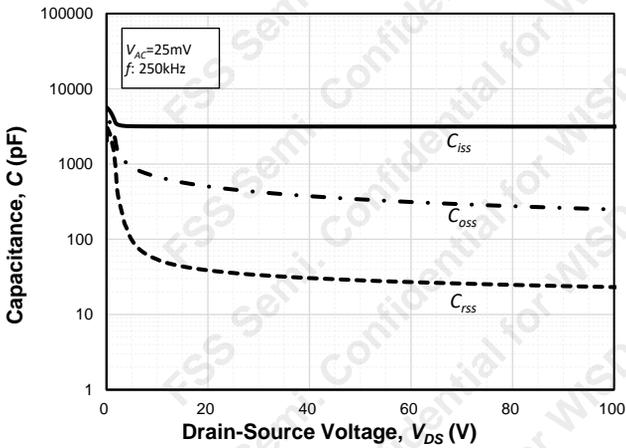


Fig. 15 Typ. Capacitance vs. V_{DS} at $f_{sw} = 250\text{kHz}$, $V_{DS} \leq 100\text{V}$

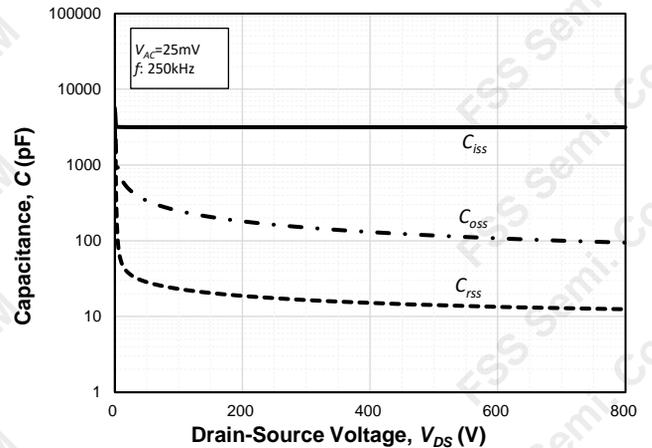


Fig. 16 Typ. Capacitance vs. V_{DS} at $f_{sw} = 250\text{kHz}$, $V_{DS} \leq 800\text{V}$

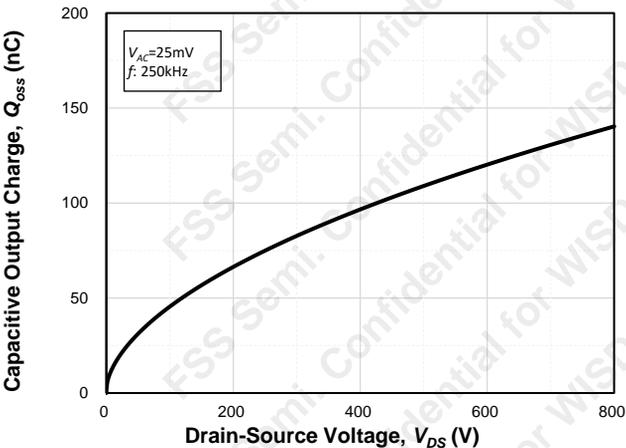


Fig. 17 Typ. Capacitive Output Charge at $f_{sw} = 250\text{kHz}$

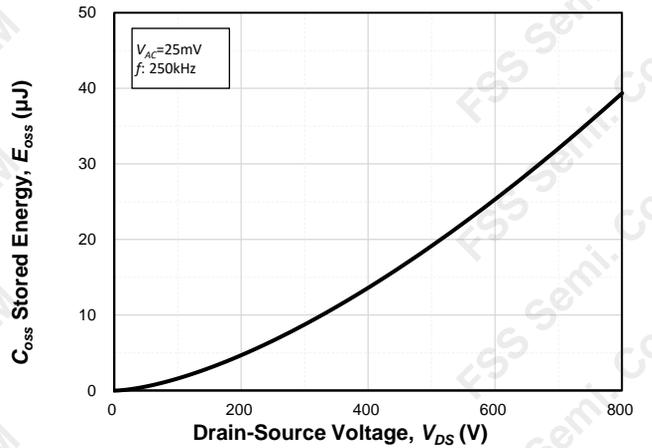


Fig. 18 Typ. C_{oss} Stored Energy at $f_{sw} = 250\text{kHz}$

Electrical Characteristics Diagrams

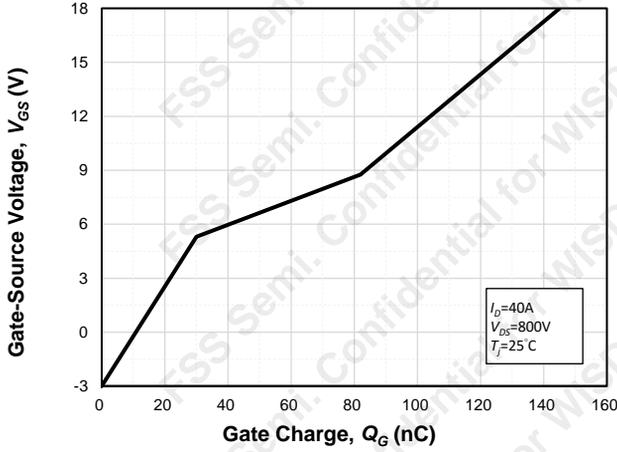


Fig. 19 Typ. Gate Charge at $V_{DS}=800V$, $I_D=40A$

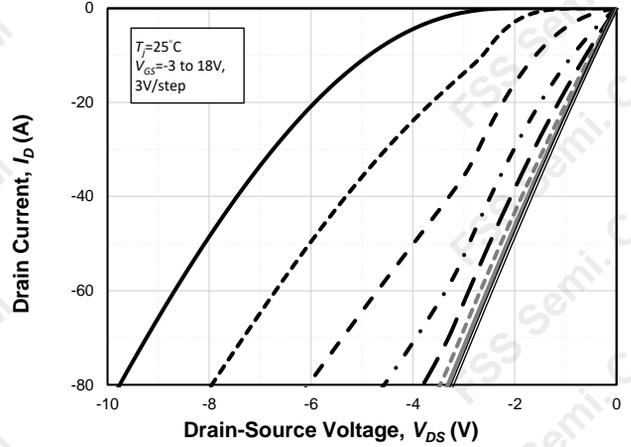


Fig. 20 Typical Forward Characteristics of Reverse Conduction at $T_J=25^\circ C$

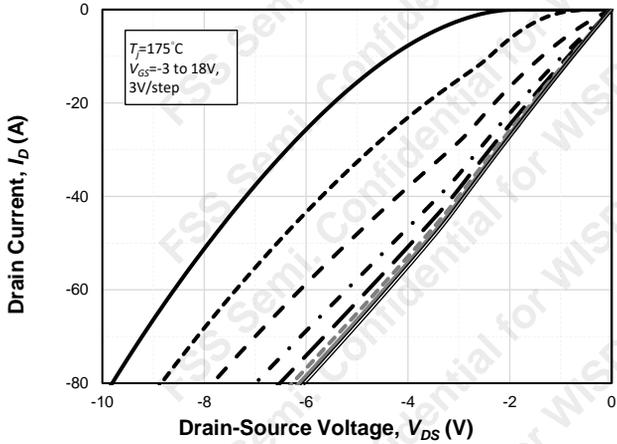


Fig. 21 Typical Forward Characteristics of Reverse Conduction at $T_J=175^\circ C$

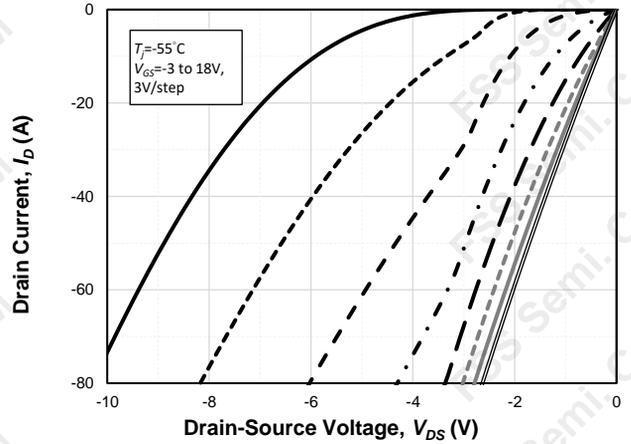


Fig. 22 Typical Forward Characteristics of Reverse Conduction at $T_J=-55^\circ C$

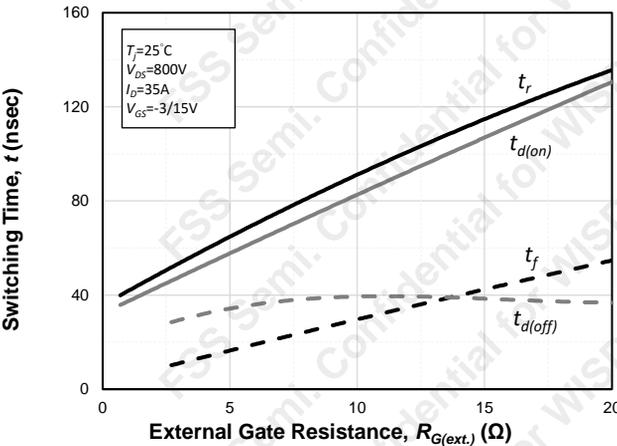


Fig. 23 Typ. Switching Time vs. $R_{G(ext.)}$

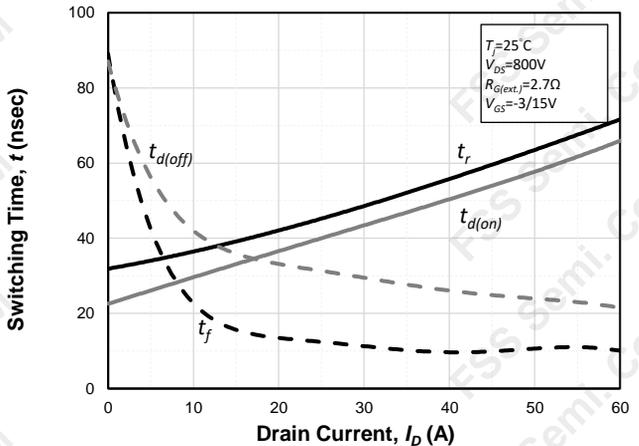


Fig. 24 Typ. Switching Time vs. I_D

Electrical Characteristics Diagrams

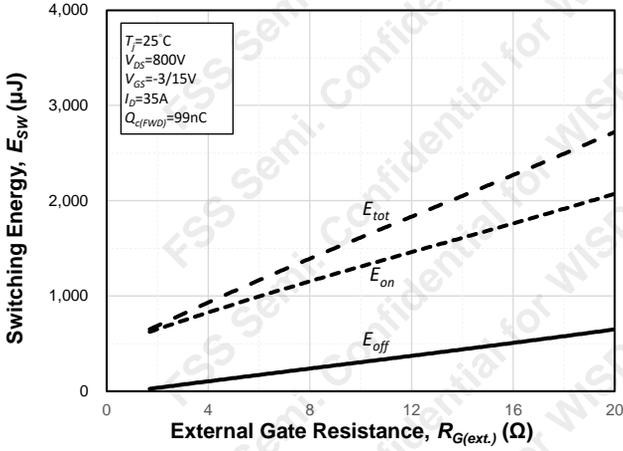


Fig. 25 Typ. Switching Energy vs. $R_{G(ext.)}$

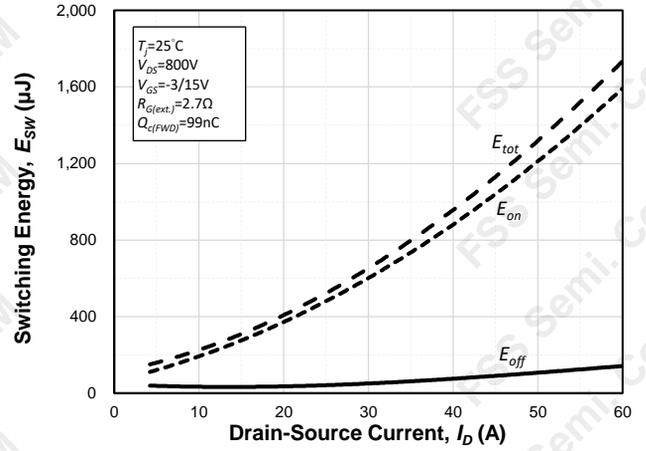
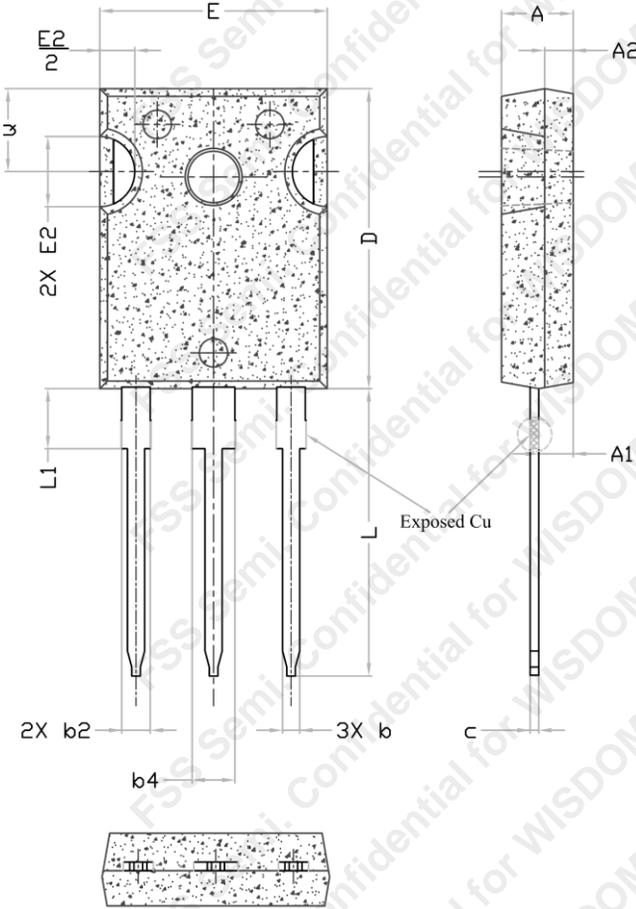


Fig. 26 Typ. Switching Energy vs. I_D

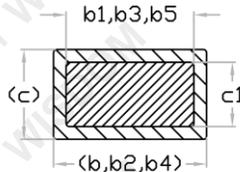
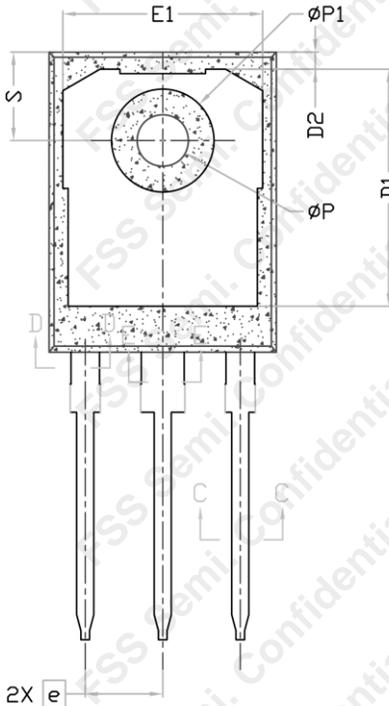
Package Outline (TO-247-3L)



Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	4.83	5.02	5.21
A1	2.29	2.41	2.55
A2	1.50	2.00	2.49
b	1.12	1.20	1.33
b1	1.12	1.20	1.28
b2 ⁽⁴⁾	1.91	2.00	2.39
b3	1.91	2.00	2.34
b4 ⁽⁴⁾⁽⁶⁾	2.87	3.00	3.22
b5	2.87	3.00	3.18
c ⁽⁴⁾	0.55	0.60	0.69
c1	0.55	0.60	0.65
D ⁽²⁾	20.80	20.95	21.10
D1 ⁽³⁾	16.25	16.55	17.65
D2	0.51	1.19	1.35
E ⁽²⁾	15.75	15.94	16.13
E1 ⁽³⁾	13.46	14.02	14.16
E2 ⁽¹⁾	4.32	4.91	5.49
e	5.44 BSC.		
L	19.81	20.07	20.32
L1 ⁽⁴⁾	4.10	4.19	4.40
φP ⁽⁵⁾	3.56	3.61	3.65
φP1	7.19 REF.		
Q	5.39	5.79	6.20
S	6.04	6.17	6.30

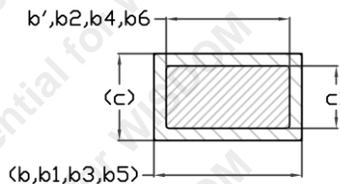
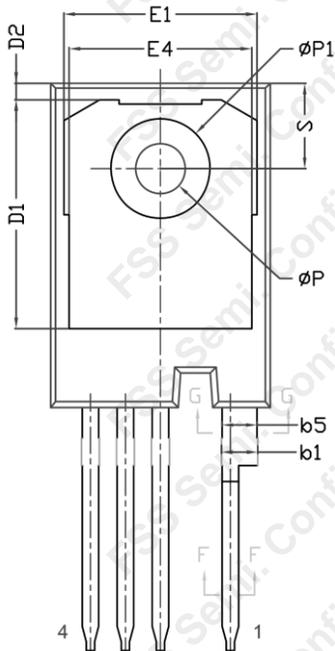
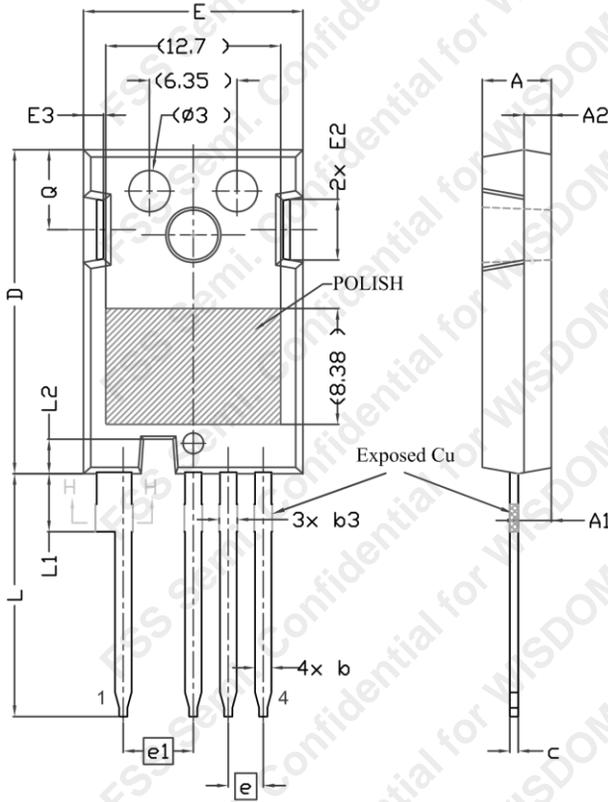
Note:

1. Slot required, notch may be rounded.
2. Dimension D & E do not include mold flash. Mold flash shall not exceed 0.127mm pre side. These dimensions are measured at the outermost extreme of the plastic body.
3. Thermal pad contour optional within dimension D1 & E1.
4. Lead finish uncontrolled in L1.
5. φP to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91mm.
6. Dimension "b2" and "b4" does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of "b2" and "b4" dimension at maximum material condition.



Section C--C,D--D,E--E

Package Outline (TO-247-4L)

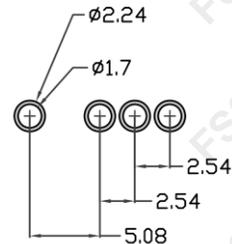


Section F-F, G-G, H-H

Symbol	Dimension (Millimeters)		
	Min.	Nom.	Max.
A	4.83	5.02	5.21
A1	2.29	2.41	2.54
A2	1.91	2.00	2.16
b'	1.07	1.20	1.28
b	1.07	1.20	1.33
b1	2.39	2.67	2.94
b2	2.39	2.67	2.84
b3	1.07	1.30	1.60
b4	1.07	1.30	1.50
b5	2.39	2.53	2.69
b6	2.39	2.53	2.64
c	0.55	0.60	0.68
c1	0.55	0.60	0.65
D	23.30	23.45	23.60
D1	16.25	16.55	17.65
D2	0.95	1.19	1.25
E	15.75	15.94	16.13
E1	13.10	14.02	14.15
E2	3.68	4.40	5.10
E3	1.00	1.45	1.90
E4	12.38	13.26	13.43
e	2.54 BSC.		
e1	5.08 BSC.		
L	17.31	17.57	17.82
L1	3.97	4.19	4.37
L2	2.35	2.50	2.65
øP	3.51	3.61	3.65
øP1	7.19 REF.		
Q	5.49	5.79	6.00
S	6.04	6.17	6.30

Note:

1. Slot required, notch may be rounded.
2. Dimension D & E do not include mold flash. Mold flash shall not exceed 0.127mm pre side. These dimensions are measured at the outermost extreme of the plastic body.
3. Thermal pad contour optional within dimension D1 & E1.
4. Lead finish uncontrolled in L1.
5. øP to have a maximum draft angle of 1.5° to the top of the part with a maximum hole diameter of 3.91mm.



Recommended Solder Pad Layout

Revision History

Date	Revision	Changes
21.07	Tentative	1 st issue
22.09	Preliminary	Update to preliminary version
23.02	Preliminary	Update switching and relative characteristics
23.04	Preliminary	Update parameter

Important Note (Disclaimer)

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This product is not designed or intended for use for applications in which the failure of the product could lead to personal injury, death or property damage, including but not limited to equipment used in medical systems, traffic communication or control systems, transportations (cars, ships, trains) and aerospace. FSS shall have no responsibility for any damages or injury arising from non-compliance with the recommended usage conditions provided herein.

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Hsinchu, Taiwan
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